UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/531,141	08/29/2005	Giovanni Tricomi	1001/0166PUS1	5064

60601 7590 11/30/2010

Muncy, Geissler, Olds & Lowe, PLLC
4000 Legato Road
Suite 310
FAIRFAX, VA 22033

EXAMINER	
HUBER, ROBERT T	

ART UNIT	PAPER NUMBER
2892	

MAIL DATE	DELIVERY MODE
11/30/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/531,141	TRICOMI ET AL.	
	Examiner	Art Unit	
	ROBERT HUBER	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-8,13-17 and 24-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-8,13-17 and 24-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2008* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114 was filed in this application after appeal to the Board of Patent Appeals and Interferences, but prior to a decision on the appeal. Since this application is eligible for continued examination under 37 CFR 1.114 and the fee set forth in 37 CFR 1.17(e) has been timely paid, the appeal has been withdrawn pursuant to 37 CFR 1.114 and prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on September 29, 2010 has been entered.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the plastic material encapsulating the semiconductor die, pedestals, one end of the terminal finger, and first and second bond wires of claim 37 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet,

and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 32 – 40 are objected to because of the following informalities: Claim 32, lines 14 – 15 recited "*said die height*", which lacks proper antecedent basis, and should read "*said semiconductor die height*". Claims 33 – 40 depend from claim 32. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 2 – 7, 13, 14, 16, 17, 24, 25, 28 and 31 - 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pritchard et al. (US 5,479,050, prior art of record) in view of Kwon et al. (US 5,365,409, prior art of record).

a. Regarding claim 16, **Prichard discloses an integrated circuit device** (e.g. figures 1 – 3), **comprising:**

a semiconductor die (die 11);

a carrier device comprising a die paddle having a support surface onto which the semiconductor die is attached (die paddle 16, disclosed in col. 1, line 65, which is the support surface portion of leadframe 10 under semiconductor die 11), **and a plurality of stamped pedestals** (pedestals 12 and 13, disclose in col. 1, lines 65 – 67 to be stamped) **arranged on a metal layer extending in a device plane exteriorly surrounding and adjacent to the die paddle** (e.g. as seen in figure 1, the pedestals 12 and 13 on the metal layer of the leadframe 10 in the plane of the device and exteriorly surround and are adjacent to the top of the die paddle region under the semiconductor die 11),

wherein the carrier device, the die paddle and the stamped pedestals form a single piece unitary structure (e.g. as seen in the figure, the carrier device, die paddle, and stamped pedestals are formed from a single piece);

a plurality of leads (leads 17 and 18) **each comprising an inner lead portion** (inner portion towards the die) **that extends to an outer lead portion** (outer portion furthest away from the die); **and**

a first bond wire extending from the die to a first of the plurality of stamped pedestals (bond wire 15)**, and a second bond wire extending to an inner lead portion** (bond wire 22),

wherein at least one of said stamped pedestals includes a sidewall having a face extending, upward from the device plane, from a pedestal base junction extending along a closed path on the device plane, to a pedestal top surface spaced a pedestal height above the device plane, the sidewall being continuous, at all points of the pedestal base junction, from the pedestal base junction to the pedestal top surface (as clarified in the figure below, the sidewall of the stamped pedestal extends upward from the device plane of the leadframe 10, and is continuous since there are no breaks in the sidewall or at the junction of the sidewall and the base. Regarding the closed path, any path may be chosen at the pedestal base junction such that it is a closed path).

Pritchard is silent with respect to explicitly disclosing that the plurality of leads are metallic, the second bond wire extends from the first

of the plurality of stamped pedestals to the inner lead portion, and a package that encapsulates the semiconductor die, the die paddle, the first and second bond wires and the inner lead portions.

Kwon discloses an integrated circuit structure (e.g. figure 5), **comprising a first bond wire** (bond wire 160) **extending from the die** (die 154) **to a first of the plurality of pedestals** (pedestals 158), **and a second bond wire** (bond wire 162) **extending from the first of the plurality of pedestals to an inner lead portion** (inner lead portion of lead 156); **and a package that encapsulates the semiconductor die, the die paddle, the first and second bond wires and the inner lead portions** (e.g. as seen in figure 5, there is a package, denoted by a dashed line, that encapsulates the die, paddle, wires and inner lead portions).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard such that the second bond wire extends from the stamped pedestal to the inner lead portion since Pritchard discloses that electrical connections may be formed between the die, pedestals, and surrounding leads, and Kwon also discloses that electrical connections may be formed between the die, pedestals, and surrounding leads such that a first bond wire connects the semiconductor die to a pedestal, and second bond wire connects the pedestal to a lead finger. One would have been motivated to form a wire bond between the semiconductor die and the pedestal, and between the pedestal and the inner portion of the lead in order to relieve the

wire bond of stress formed by making a direct connection between the semiconductor die and the inner portion of the lead.

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard such that a package encapsulates the die, die paddle, inner lead portions, and bond wires since it was well known in the art that semiconductor structures are encapsulated in such a manner, as supported by Kwon. One would have been motivated to encapsulate the structure in order to protect the inner device elements from external stresses.

Furthermore, although Pritchard does not explicitly disclose forming the surrounding leads from metal, it would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard such that the surrounding leads were formed from metal since Pritchard discloses connecting the leads to the die via wire bonds to form an electrical circuit, and it has been held that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. See MPEP 2144.07. One would have been motivated to use metal for the surrounding leads since it is electrically conductive, durable, and inexpensive.

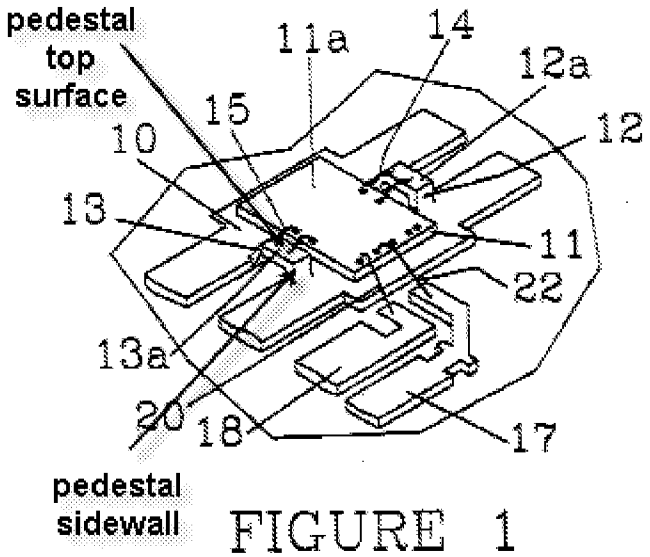

FIGURE 1

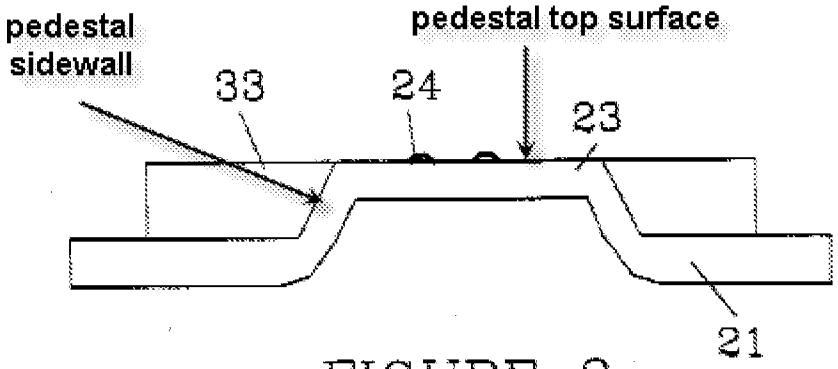

FIGURE 3

b. Regarding claim 17, **Pritchard discloses an integrated circuit** (e.g. figure 1), **comprising:**

a semiconductor die (die 11);

a carrier device comprising a planar surface onto which the semiconductor die is attached (carrier device 16, disclosed in col. 1, line 65,

which is the portion of leadframe 10 under semiconductor die 11), **and a plurality of stamped pedestals** (pedestals 12 and 13, disclose in col. 1, lines 65 – 67 to be stamped) **arranged on a metal layer extending in a device plane exteriorly surrounding and adjacent to the planar surface** (e.g. as seen in figure 1, the pedestals 12 and 13 on the metal layer of the leadframe 10 in the plane of the device and exteriorly surround and are adjacent to the top of the die paddle region under the semiconductor die 11), **wherein the carrier and the stamped pedestals form a single piece unitary structure** (e.g. as seen in the figure, the carrier device and stamped pedestals are formed from a single piece);

a plurality of leads (leads 17 and 18) **each comprising an inner lead portion** (inner portion towards the die) **that extends to an outer lead portion** outer portion furthest away from the die); **and**

a first bond wire extending from the die to a first of the plurality of stamped pedestals (bond wire 15)**, and a second bond wire extending to an inner lead portion** (bond wire 22),

wherein at least one of said stamped pedestals includes a sidewall having a face extending, upward from the device plane, from a pedestal base junction extending along a closed path on the device plane, to a pedestal top surface spaced a pedestal height above the device plane, the sidewall being continuous, at all points of the pedestal base junction, from the pedestal base junction to the pedestal top surface (as clarified in the figure above, the sidewall of the stamped pedestal extends upward from the

device plane of the leadframe 10, and is continuous since there are no breaks in the sidewall or at the junction of the sidewall and the base. Regarding the closed path, any path may be chosen at the pedestal base junction such that it is a closed path).

Pritchard is silent with respect to explicitly stating that the carrier device and the plurality of leads are "metallic", and the second bond wire extends from the first of the plurality of stamped pedestals to the inner lead portion.

Kwon discloses an integrated circuit structure (e.g. figure 5), **comprising a first bond wire** (bond wire 160) **extending from the die** (die 154) **to a first of the plurality of pedestals** (pedestals 158), **and a second bond wire** (bond wire 162) **extending from the first of the plurality of pedestals to an inner lead portion** (inner lead portion of lead 156).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard such that the second bond wire extends from the stamped pedestal to the inner lead portion since Pritchard discloses that electrical connections may be formed between the die, pedestals, and surrounding leads, and Kwon also discloses that electrical connections may be formed between the die, pedestals, and surrounding leads such that a first bond wire connects the semiconductor die to a pedestal, and second bond wire connects the pedestal to a lead finger. One would have been motivated to form a wire bond between the semiconductor die and the pedestal,

and between the pedestal and the inner portion of the lead in order to relieve the wire bond of stress formed by making a direct connection between the semiconductor die and the inner portion of the lead.

It would have been obvious for one of ordinary skill in the art at the time the invention was made to use a metallic material in the carrier device of Pritchard, since Pritchard discloses connecting leads to the carrier device (stamped pedestals) to form an electrical circuit, and it has been held by the courts that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. *In re Leshin*, 125 USPQ 416 (CCPA 1960) and *Sinclair & Carroll Co. v. Interchemical Corp.*, 65 USPQ 297 (1945). One would have been motivated to make the carrier device metallic in order to create a conductive portion of the carrier to complete an electrical circuit, as well as allowing the pedestals to be formed easily by stamping.

Furthermore, although Pritchard does not explicitly disclose forming the surrounding leads from metal, it would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard such that the surrounding leads were formed from metal since Pritchard discloses connecting the leads to the die via wire bonds to form an electrical circuit, and it has been held that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. See MPEP 2144.07. One would have been motivated to use metal for the surrounding leads since it is electrically conductive, durable, and inexpensive.

c. Regarding claim 2, **Pritchard in view of Kwon disclose the integrated circuit device of claim 16, as cited above, wherein a plane of the carrier device die paddle is in said device plane** (as seen in figures 1 and 3, the device plane and the carrier plane have a common plane), **and wherein the stamped pedestals have sidewalls with an angle (α) greater than 45 degrees with respect to a plane of the carrier device die paddle** (e.g. figures 1 and 3 of Pritchard show the angle of the pedestal sidewall has an angle of 90 (figure 1) and greater than 45 degrees (figure 3) with respect to the top or bottom plane of the die paddle).

d. Regarding claim 3, **Pritchard in view of Kwon disclose the integrated circuit device of claim 16, as cited above, wherein the top surface of the stamped pedestals each have a plane surface which is parallel to a chip connection area plane of the carrier device** (e.g. as seen in figure 3 of Pritchard) **and each has an area for connection of a single bonding wire** (e.g. as seen in figure 1 of Pritchard, there is an area surrounding the bond wire connection on the pedestals 12 and 13 for connecting a single bond wire 14 or 15).

e. Regarding claim 4, **Pritchard in view of Kwon disclose the integrated circuit device of claim 16, as cited above, wherein said pedestal height of**

each of the stamped pedestals lies in the range between 1/10 and 1.5 times the height of the semiconductor die (as seen in figure 3 and disclosed in col. 2, lines 15 - 17 of Pritchard, the stamped pedestals have a height the same as the semiconductor die, and therefore are within the claimed range).

f. Regarding claim 5, **Pritchard in view of Kwon disclose the integrated circuit device of claim 16, as cited above, but is silent with respect to said pedestal height of each of the raised pedestals lies in the range from 1/5 to twice a material thickness (h) of the carrier device. Pritchard and Kwon show that the height of the pedestal may be about 0.5 times the height of the carrier device, but it is not explicitly stated.**

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard in view of Kwon such that the pedestals are within the range of 1/5 to 2 times the carrier device thickness, since Pritchard and Kwon suggests through the figure this may be the case, and it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only ordinary skill in the art. *In re Aller*, 105 USPQ 233. One would have been motivated to make the height of the pedestal within the range of the carrier device in order to reduce lead length and stress on the leads.

g. Regarding claims 6 and 7, **Pritchard in view of Kwon discloses the structural limitations of the integrated circuit device, as cited in claim 16. The process by which the raised pedestal is formed is not given patentable weight since the patentability of a product does not depend on the method of production. See MPEP 2113.**

h. Regarding claim 13, **Pritchard in view of Kwon discloses the integrated circuit device of claim 17, as cited above, wherein the sidewalls of the stamped pedestals make an angle (α) greater than 45 degrees with the device plane of the carrier device** (e.g. figures 1 and 3 of Pritchard show the angle of the pedestal sidewalls have an angle of 90 (figure 1) and greater than 45 degrees (figure 3) with respect to the top or bottom plane of the die paddle).

Pritchard and Kwon are silent with respect to explicitly stating the sidewalls have at their base rounded junctions with the device plane.

However, it would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard in view of Kwon such that the sidewalls of the pedestals to have rounded junctions with the device plane, since it has been held by the courts that a change in shape or configuration, without any criticality, is nothing more than one of numerous shapes that one of ordinary skill in the art will find obvious to provide based on the suitability for the intended final application. See *In re Dailey*, 149 USPQ 47

(CCPA 1976). It appears that the disclosed device of Kwon would perform equally well shaped as disclosed by the Applicant. One would have been motivated to have rounded pedestals since materials deposited often have rounded edges due to the formation process.

i. Regarding claim 14, **Pritchard in view of Kwon disclose the integrated circuit device of claim 17, as cited above, wherein the height of the stamped pedestals lies in the range between 1/10 to one time the die height** (as seen in figure 3 and disclosed in col. 2, lines 15 - 17 of Pritchard, the stamped pedestals have a height the same as the semiconductor die).

j. Regarding claims 24 and 25, **Pritchard in view of Kwon disclose the integrated circuit device of claims 16 and 17, as cited above respectively, wherein the metallic leads are separate from the metallic carrier device** (e.g. as seen in figure 1 of Pritchard, the leads 17 and 18 are separate from the carrier device 16).

k. Regarding claims 28 and 31, **Pritchard in view of Kwon disclose the integrated circuit device of claims 16 and 17, as cited above respectively, wherein said semiconductor die has a side surface extending from the bottom surface to the top surface** (e.g. as seen in figures 1 and 3 of Pritchard and figure 5 of Kwon), **said side surface extending along a rectangular**

perimeter lying in said device plane (e.g. as seen in figures 1 and 2 of Pritchard, side surface of semiconductor die 11 has rectangular perimeter in device plane), **said rectangular perimeter having a first side** (e.g. first side of die 11 closed to leads 17 and 18 of Pritchard), **a second side parallel to and spaced from said first side** (Pritchard: second side of die 11 close to pedestal 13), **and a third side normal to said first side** (Pritchard: third side of die 11 close to pedestal 12), **wherein each of said plurality of said stamped pedestals is located adjacent said first side** (as seen in figure 1 of Pritchard, the plurality of pedestals 12 and 13 are adjacent (close to or near) the first side of die 11).

l. Regarding claim 32, **Pritchard discloses an integrated circuit device** (e.g. figures 1 – 3), **comprising:**

a carrier having a die support surface extending in a support plane (carrier 10 with die support surface and plane under semiconductor die 11), **and a plurality of pedestals surrounding and adjacent to the die support surface** (pedestals 12 and 13, disclose in col. 1, lines 65 – 67), **each pedestal projecting a pedestal height above the support plane** (e.g. as seen in figures 1 and 3);

a semiconductor die attached to the die support surface of the carrier (semiconductor die 11, col. 1, line 64), **having a top surface located a die height above the support plane** (e.g. as seen in figures 1 and 3, top

surface of die 11), **and a plurality of bond pads on an area of the top surface** (as seen in figures 1 and 2, bond pads 22 are on top surface of die 11 to which bond wires, e.g. 14 and 15, are attached, col. 2, lines 31 - 32);

a lead finger supported to have one end proximal at least one of said pedestals, extending away from the semiconductor die (e.g. lead finger 18 with inner end proximal (situated close to) pedestal 13);

a first bond wire extending from one of said bond pads to one of said at least one pedestals proximal the one end of the lead finger (e.g. bond wire 15).

Pritchard is silent with respect to disclosing a second bond wire extending from said one of said pedestals to said one end of said lead finger, wherein said pedestal height is in the range between 1/5 and 1/2 of said semiconductor die height (see claim objection above). **Pritchard discloses the pedestal height is about the same height as the semiconductor die, as seen in figure 3.**

Kwon discloses an integrated circuit structure (e.g. figure 5), **comprising a first bond wire** (bond wire 160) **extending from the die** (die 154) **to a first of the plurality of pedestals** (pedestals 158), **and a second bond wire** (bond wire 162) **extending from the first of the plurality of pedestals to a lead finger** (lead 156), **wherein said pedestal height is in the range between 1/5 and 1/2 of the semiconductor die height** (as seen in figure 5, the height of the pedestal 158 is about 1/2 the height of the die 154)

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard such that the second bond wire extends from the pedestal to the end of the lead finger since Pritchard discloses that electrical connections may be formed between the die, pedestals, and surrounding leads, and Kwon also discloses that electrical connections may be formed between the die, pedestals, and surrounding leads such that a first bond wire connects the semiconductor die to a pedestal, and second bond wire connects the pedestal to a lead finger . One would have been motivated to form a wire bond between the semiconductor die and the pedestal, and between the pedestal and the lead finger in order to relieve the wire bond of stress formed by making a direct connection between the semiconductor die and the inner portion of the lead.

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard in view of Kwon such that the pedestal height is within the range of 1/5 to 1/2 times the semiconductor die height, since Kwon suggests through the figure this may be the case, and it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only ordinary skill in the art. *In re Aller*, 105 USPQ 233. One would have been motivated to make the height of the pedestal within the range of the semiconductor die height in order to reduce lead length and stress on the leads.

m. Regarding claim 33, **Pritchard in view of Kwon disclose the integrated circuit device of claim 32, wherein at least one of the pedestals has a pedestal top planar surface located at the pedestal height of said at least one pedestal above the support plane** (Pritchard: e.g. top surface 13a of pedestal 13 is at a pedestal height above the support plate between the die 11 and carrier 10).

n. Regarding claim 34, **Pritchard in view of Kwon disclose the integrated circuit device of claim 33, wherein said first bond wire and said second bond wire each attach to said pedestal top planar surface** (Kwon: as seen in figure 5, first bond wire 160 and second bond wire 162 are attached to the pedestal 158 top planar surface).

o. Regarding claim 35, **Pritchard in view of Kwon disclose the integrated circuit device of claim 32, wherein the die support surface is a surface of a portion of a carrier platform structure** (Pritchard: as seen in the figures), **and at least one of the pedestals comprises a pedestal structure attached to the carrier platform structure** (Pritchard: as seen in figures, the pedestals 12 and 13 attach to the carrier platform structure of carrier 10).

p. Regarding claim 36, **Pritchard in view of Kwon disclose the integrated circuit device of claim 32, wherein all of the pedestals have the same**

pedestal height (as rendered obvious by figures 1 and 3 of Pritchard and figure 5 of Kwon).

q. Regarding claim 37, **Pritchard in view of Kwon disclose the integrated circuit device of claim 32, further comprising a plastic material encapsulating said semiconductor die, said pedestals, said one end of the terminal finger, said first bond wire and said second bond wire** (as seen with respect to figures 1 and 5 of Kwon, plastic material 30 encapsulates the die, pedestals, fingers, bond wires, disclosed in col. 2, lines 20 – 23. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard in view of Kwon such that a plastic material encapsulated the structure since it was well-known in the art to encapsulate the leads, bond wires, pedestals and die, for at least the reason of protecting the leads, bond wires, pedestals, and die from damage and electrical shorting).

r. Regarding claim 38, **Pritchard in view of Kwon disclose the integrated circuit device of claim 37. Pritchard and figure 5 of Kwon are silent with respect to disclosing the device having a non-bonded pedestal, said non-bonded pedestal having no bond wire attached, and having one continuous laminated structure with a first portion forming said die support and a second portion forming said non-bonded pedestal.**

Figure 4 of Kwon discloses that a non-bonded intermediate lead (110) **having no bond wire attached** (as seen in figure 4, there are intermediate leads 110 with bond wires 112 and 116 attached, and intermediate least 110 without bond wires attached).

Therefore, it would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard in view of Kwon such that there was a non-bonded pedestal since it was known in the art that intermediate contacts (leads and pedestals) may remain un-bonded within the leadframe device structure, as shown in figure 4 of Kwon. One would have been motivated to modify the device of Pritchard in view of Kwon depending on circuit design and semiconductor chip structure, thereby allowing the use of different semiconductor chip connections with the same leadframe structure. Since different chips may have different bond pads, some pedestals may be bonded with certain chip structures, while others may remain un-bonded.

The non-bonded pedestal structure of Kwon renders obvious the structure of having one continuous laminated structure with a first portion forming said die support and a second portion forming said non-bonded pedestal, as seen with the unitary pedestal and carrier structure of Pritchard (e.g. figure 1)

7. Claims 8, 15, 26, 27, 29, 30, 39, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pritchard in view of Kwon, and in further view of Carter, Jr. et al. (US 6,365,976 B1, prior art of record).

a. Regarding claim 8, **Pritchard in view of Kwon disclose the integrated circuit device of claim 16, but are silent with respect to a silver or gold finish is on the stamped pedestals.**

Carter discloses that gold or silver finishes may be applied to raised pedestals in integrated circuits (Col. 5, lines 18 - 22, disclose that the surface of the pedestals have a foil on them which may consist of silver or gold, or the pedestal may be covered with a tin-silver layer).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard in view of Kwon such that there is a gold or silver finish on the raised pedestals since it was known in the art that such pedestals in integrated circuits my have a finish applied to them, as disclosed by Carter. One would have been motivated to have a gold or silver finish applied to the pedestals since gold and silver promote the bonding of the wires to the pedestals and are highly conductive.

b. Regarding claim 15, **Pritchard in view of Kwon disclose an integrated circuit device of claim 16, as cited above, but are silent with respect to disclosing only in the areas of the stamped pedestals, a finish, having at least one of silver or gold, is provided for bondability.**

Carter discloses that areas of pedestals may be provided with a gold or silver finish (col. 5, lines 20 - 22, discloses that the pedestal ("dimple") may covered with a layer of tin-silver).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard in view of Kwon such that there is a gold or silver finish on the raised pedestals since it was known in the art that such pedestals in integrated circuits my have a finish applied to them, as disclosed by Carter. One would have been motivated to have a gold or silver finish applied to the pedestals since gold and silver promote the bonding of the wires to the pedestals and are highly conductive.

c. Regarding claims 26 and 29, **Pritchard in view of Kwon disclose the integrated circuit device of claims 16 and 17, as cited above respectively, wherein said semiconductor die has a side surface extending from a bottom surface to a top surface** (e.g. as seen in figures 1 and 3 of Pritchard and figure 5 of Kwon**), said side surface extending along a rectangular perimeter lying in the device plane** (as seen in figure 1 and 2 of Pritchard), **said rectangular perimeter having a first side** (e.g. left side of die 11 close to pedestal 13 in figure 1 of Pritchard), **a second side parallel to and spaced from said first side (**e.g. right side of die 11 close to pedestal 12 in figure 1 of Pritchard), **and a third side normal to said first side** (e.g. side of die 11 close to leads 17 and 18 in figure 1 of Pritchard), **wherein a first of said stamped**

pedestals is located adjacent said first side (e.g. pedestal 13 of Pritchard), **a second of said stamped pedestals is located adjacent said second side** (e.g. pedestal 12 of Pritchard).

Pritchard and Kwon are silent with respect to explicitly disclosing a third of said stamped pedestals is located adjacent said third side.

Carter discloses (as seen in with respect to figures 1B, 1C, 2B and 3F) **the semiconductor die** (306) **is surrounded by pedestals** (e.g. as seen in figures 1B and 1C, pedestals 112 and 121), **such that the pedestals are located adjacent a first, second, third, and fourth side of the semiconductor die** (as seen in with respect to figures 1C and 3F).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard in view of Kwon such that third of said stamped pedestals is located adjacent said third side of the semiconductor die since Pritchard and Kwon explicitly disclose forming pedestals on two sides of the semiconductor die, and Carter explicitly discloses that pedestals may be formed on all four sides of the semiconductor die. One would have been motivated to form a pedestal located adjacent the third side of the semiconductor die in order to help alleviate stresses in the bond wires extending from the third side of the semiconductor die, as well as enhance the conductivity of the device.

d. Regarding claims 27 and 30, **Pritchard in view of Kwon and Carter disclose the integrated circuit device of claims 26 and 29, as cited above respectively, wherein said semiconductor die has a further side surface parallel to and spaced from said third side surface, and wherein at least one of said stamped pedestals is located adjacent said fourth side** (as cited above with respect to claims 26 and 29, Carter renders obvious forming the pedestals on all sides of the semiconductor die, and hence Pritchard in view of Kwon and Carter render obvious forming a stamped pedestal adjacent the fourth side of the semiconductor die, for at least the reason of helping to alleviate stresses in the bond wires extending from the fourth side of the semiconductor die).

e. Regarding claims 39 and 40, **Pritchard in view of Kwon disclose the integrated circuit of claim 33, but are silent with respect to disclosing portions of said carrier have a first finish and said planar top surfaces have a second finish different from said first finish, wherein said second finish includes a metal from the group consisting of gold and silver.**

Carter discloses that areas of pedestals may be provided with a gold or silver finish (col. 5, lines 20 - 22, discloses that the pedestal ("dimple") may covered with a layer of tin-silver) **to a carrier made of a different metal material** (col. 5, lines 10 - 15).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard in view of Kwon such that there is a gold or silver finish on the raised pedestals since it was known in the art that such pedestals in integrated circuits my have a finish applied to them, as disclosed by Carter. One would have been motivated to have a gold or silver finish applied to the pedestals since gold and silver promote the bonding of the wires to the pedestals and are highly conductive.

The formation of gold or silver finish on the raised pedestals renders obvious the structural limitation of said carrier have a first finish and said planar top surfaces have a second finish different from said first finish, since the planar top surfaces of the raised pedestals will have a gold or silver finish, while the remaining carrier may have a copper or aluminum finish, as discussed by Carter (col. 5, lines 10 - 15 and lines 18 - 22).

Response to Arguments

8. Applicant's arguments filed on September 29, 2010 have been fully considered but they are not persuasive. At present, the prior art of Pritchard et al. in view of Kwon et al. remains commensurate to the scope of the claims as stated by the Applicant within the context of the claim language and as broadly interpreted by the Examiner [MPEP 2111], which is elucidated and expounded upon above. In response to Applicants arguments drawn to the amendment to claims 16 and 17 of "*at least one of said stamped pedestals includes a sidewall having a face extending, upward from the*

device plane, from a pedestal base junction extending along a closed path on the device plane, to a pedestal top surface spaced a pedestal height above the device plane, the sidewall being continuous, at all points of the pedestal base junction, from the pedestal base junction to the pedestal top surface", the Examiner submits that the prior art of Pritchard discloses such a claimed structure. The Applicant argues that Pritchard discloses an inherently discontinuous pair of separate base junctions and discontinuous pair of opposing, separate sidewalls (see page 11 of Remarks). The Examiner recognizes the structure of Pritchard as discussed by the Applicant, however, under a broad, reasonable interpretation, the Examiner finds that the claimed structure, as cited above, reads on the invention of Pritchard. In particular, as clarified above with respect to claims 16 and 17, one may interpret the side wall of the pedestal 12 or 13 of Pritchard as that indicated in the figure above. As seen in the figure, the sidewall ahs a face extending upwards from the device plane and from a base junction. Regarding a closed path on the device plane, one may choose any path of the sidewall on the plane to be a "closed" path, and therefore a closed path may be chosen within the pedestal sidewall on the device plane. Clearly, Pritchard shows the sidewall of pedestal 12 or 13 extending to a top surface 12a or 13a, respectively. One may consider the sidewall as interpreted to be continuous since there are no holes, breaks, etc...within the interpreted sidewall base junction and the base junction to the top surface. Therefore, under a broad, reasonable interpretation, the Examiner finds that Pritchard et al. in view of Kwon et al. still renders obvious the claimed structure.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT HUBER whose telephone number is (571)270-3899. The examiner can normally be reached on Monday - Friday (11am - 7pm EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Robert Huber/
Examiner, Art Unit 2892
November 22, 2010